AMC 10 Channel ADC with Dual DAC

AMC520

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KEY FEATURES

- Double width per µTCA.4
- Ten channel of ADC with 125MSPS @ 16-bit resolution utilizing AD9268 device
- Dual DAC with 250 MSPS @ 16-bit resolution utilizing MAX5878 device (this is user programmable for lower sampling rate)
- Internal clock or precision external clock from RTM/backplane/front panel clocks
- Trig in/out configurable by software (external trigger via front or port 17)
- Backplane PCIe Dual x4 or x8/Dual GbE
- Xilinx Virtex-6 FPGA in FF1759 package
- Option for QDR-II+
- AMC FCLKA, TCLKA, TCLKB, TCLKC and TCLKD are routed
- Dual SFP+ (up to 6.6Gbps)
- JTAG selectable front and backplane
- AMC.1 and AMC.2 (FPGA programmable)
- RoHS compliant

The AMC520 is a ten ADC (Analog to Digital Converter) with two DAC (Digital to Analog Converter) module compliant to the AMC.1 and AMC.2 specification. The unit has an on-board, re-configurable FPGA which interfaces directly to the GbE and PCIe bus.

The FPGA has an interface to the QDR-II+ memory (36 and 72-bit wide). This allows for large buffer sizes to be stored during processing as well as for queuing the data to the host.

The AMC520 allows for flexible external clocking as well as internal clocking. The AMC520 has a Trig in/out signal that is sourced from the front panel or port 17.

Each input/output goes to the Rear Transition Module (RTM) connector that complies with uTCA.4. Each of the ADC/DAC single ended inputs are converted to differential.

The FPGA interfaces directly to the AMC per AMC.1 and AMC.2 and also includes direct front panel interfacing via dual SFP+, raw I/O headers, and LEDs. An RS-232 port is available from the FPGA if the customer desires to implement a soft-processor in the FPGA and have a serial console.

VadaTech can modify this product to meet special customer requirements without NRE (minimum order placement is required).

AdvancedMC™

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SPECIFICATIONS

Architecture		
Physical	**Dimensions**	Double-width, Mid-Height with Full-Height option
		Width: 5.85 in. (148.5 mm)
		Depth: 7.11 in. (180.6 mm
Type	**AMC ADC**	10 ADC and Dual DAC
		16-bit resolution per port on ADC and 16-bit resolution on DAC
		External/Internal clock with Trig in/out
		QDR-II+
Standards		
µTCA	**Type**	µTCA.4 with RTM
AMC	**Type**	AMC.1 and AMC.2
Module Management	**IPMI**	IPMI Version 2.0
PCIe	**Lanes**	Dual x4 or x8
Ethernet	**GbE**	1000-BaseBX
Configuration		
Power	**AMC520**	Estimated 15W, application specific (up to 40W)
Environmental	**Temperature**	Operating Temperature: 0° to 65° C (Air flow requirement is to be greater than 400 LFM)
		Storage Temperature: -40° to +90° C
	Vibration	1G, 5-500Hz each axis
	Shock	30Gs each axis
	Relative Humidity	5 to 95 percent, non-condensing
Front Panel	**Interface Connectors**	FPGA JTAG port
		Debug/status LEDs
		16 I/O pins
		MMCX Trig in/out, clock in
		IPMI RS-232, FPGA RS-232
	LEDs	IPMI Management Control
		FPGA 8 user defined LED / 16 status LEDs / 16 PCIe signal detect LEDs
	Mechanical	Hot Swap Ejector Handle
Software Support	**Operating Systems**	Linux, Windows, Solaris and VxWorks
Other		
MTBF	MIL Handbook 217-F > TBD.	
Certifications	Designed to meet FCC, CE and UL certifications where applicable	
Standards	VadaTech is certified to both the ISO9001:2000 and AS9100B:2004 standards	
Compliance	RoHS and NEBS	
Warranty	Two (2) years.	
Trademarks and Logos	The VadaTech logo is a registered trademark of VadaTech, Inc. Other registered trademarks are the property of their respective owners. AdvancedMC™ and the AdvancedTCA™ logo are trademarks of the PCI Industrial Computers Manufacturers Group. All rights reserved. Specification subject to change without notice.	

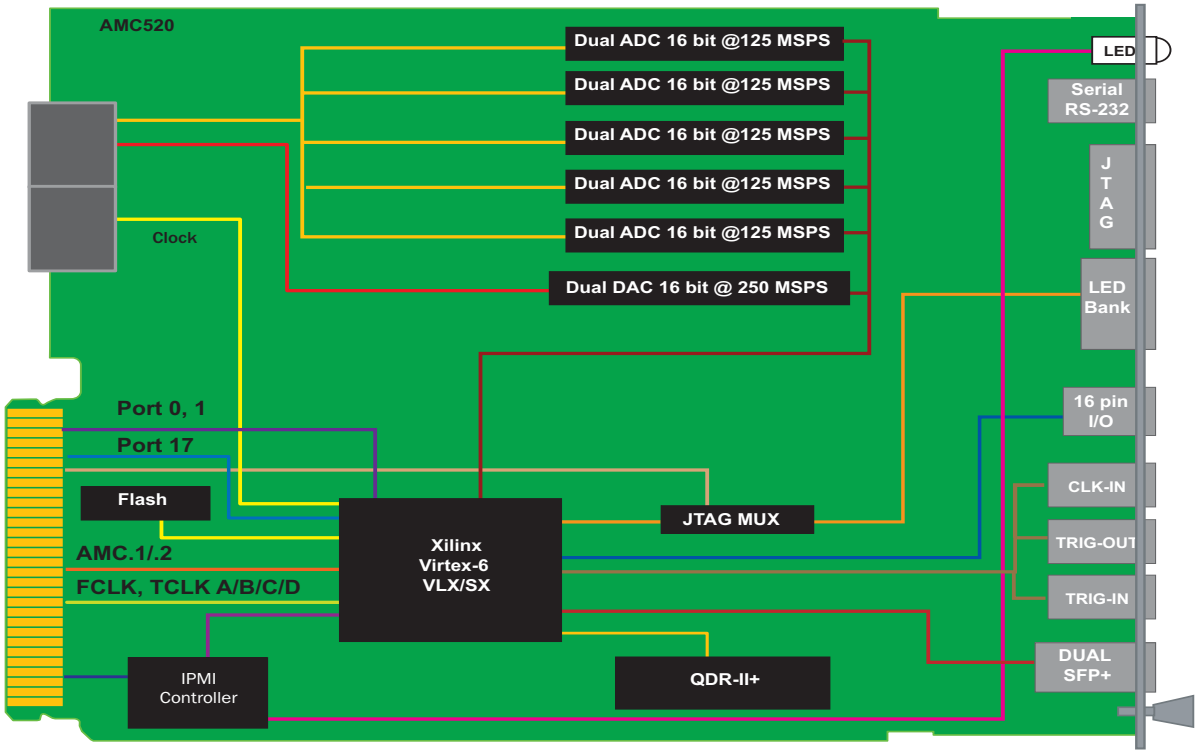

FIGURE 1. AMC520 Functional Block Diagram

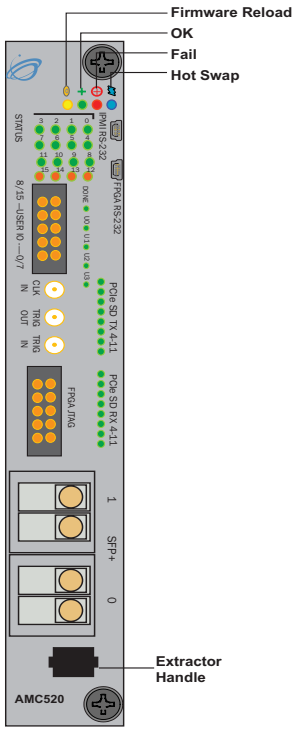

FIGURE 2. AMC520 Front Panel

ORDERING OPTIONS

AMC520 - ABC - DEF - G0J

A = QDR-II + Memory

0 = None
1 = 2 x 36 (single chip)
2 = 2 x 72 (two chips)
3 = Reserved

B = No. of ADC

1 = Reserved
2 = 10

C = Front Panel

0 = Reserved
2 = Mid-Height
3 = Full-Height

D = FPGA

1= Reserved
2= Reserved
3= Reserved
4= XC6VLX240T
5= XC6VLX365T
6= XC6VLX550T
7= XC6VSX475T
8 = Reserved

E = FPGA SPEED

1 = Low
2 = High

F = Front end A/D input via

0 = Magnetic
1 = OpAmp

G = SFP+ Transceivers*

0 = None
1 = 1Gb LC/SX (850nm)
2 = 1Gb LC/LX (1310nm)
3 = Copper 1000 Mbit (Ethernet only)
4 = 10Gb/SX
5 = 10Gb/LR

J = Conformal Coating

0 = None
1 = Humiseal 1A33 Polyurethane
2 = Humiseal 1B31 Acrylic

* The FPGA transceivers can run up to 6.6Gbps (depending on speed grade). They can not implement 10Gb Ethernet but the 10Gb transceiver is required if running another FPGA SERDES protocol that is faster than 1Gb. The transceivers and board design for the SFP+ ports are SERDES protocol agnostic unless the Copper transceivers are selected; as these have a built-in Ethernet media conversion PHY. The FPGA reference design demonstrates 1000Base-X Ethernet to the SFP+ ports.

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